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By: Heidi McCarty
Name: Heidi McCarty

SUBMISSION OF PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants enclose herewith one certified copy of a European application, Serial No. 02447125.2, filed 3 July 2002, the right of priority of which is claimed under 35 U.S.C. § 119.

Respectfully submitted,

MERCHANT & GOULD P.C.
P.O. Box 2903
Minneapolis, Minnesota 55402-0903
(612) 332-5300

Dated: 27 October 2003

By: John J. Gresens
John J. Gresens
Reg. No. 33,112

JJG:hjm

10/615,260

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Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

02447125.2

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
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Anmelder/Applicant(s)/Demandeur(s):

Q-Star Test N.V.
Lieven Bauwensstraat 20
8200 Brugge
BELGIQUE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Device for monitoring quiescent current of an electronic device

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DEVICE FOR MONITORING QUIESCENT CURRENT OF AN ELECTRONIC DEVICE

Field of the invention

[0001] The present invention is related to a device for measuring the quiescent current (I_{DDQ}) drawn by an electronic device, such as a CMOS device or an Integrated Circuit, when the device is powered by a supply voltage (V_{DD}).

State of the art

[0002] Integrated circuits need to be thoroughly tested. The current drawn by a powered CMOS device or IC, when it is not in switching mode, is called the 'quiescent current', described by the symbol I_{DDQ}. It is known that the value of this current is a very sensitive criterion for identifying possible malfunctioning of the IC. The detection of the I_{DDQ} level, and the comparison of this level with a reference, allows a straightforward pass/fail decision to be made on the quality of the device under test. Several devices and methods for I_{DDQ} measurement have been described so far.

- Document EP-A-672911 describes an I_{DDQ} test device for a CMOS device, said test device comprising a stabilized voltage source, and a current measurement circuit, which is coupled to said source.

- Document WO-A-9815844 is related to a method for inspecting an integrated circuit, wherein the supply current is measured, by measuring the voltage over a segment of the supply line through which this supply current flows.
- Document EP-A-811850 is related to a system for the measurement of a supply current of an electronic circuit, comprising a bypass switch with a dummy transistor to avoid charge transfer.
- Document EP-A-1107013 is related to a device for testing a supply connection of an electronic device, said test device comprising a current mirror.

[0003] Whatever the way in which the quiescent current is detected and/or measured, one of the major issues of I_{DDQ} measurement is that dedicated I_{DDQ} monitors must measure a very low quiescent current (in the order of microamps), while they must be able to deliver the high transient current (about a million times higher; in the order of amps) which is generated when a new test vector is applied to a Device Under Test (DUT). A test vector is defined as a digital input to the DUT, applied during a clock cycle of the DUT, and causing one or more transistors on the DUT to operate, yielding a digital output.

[0004] When the test vector is applied, the inputs of the DUT are changed, which flips the internal logic. During the switching of the logic, internal capacitances are charged and discharged, which appears as a peak in the supply current. This is usually solved employing a bypass switch, which is turned on prior to the transient spike. The bypass switch, together with the DUT decoupling capacitor C_H, ensures that the operation of the DUT is not affected during this critical period. The bypass having a low R_{ON} resistance prevents the DUT supply from dropping to

a low value, which might bring the DUT to an unknown state, as a consequence of which the test vector would no longer be valid. A power MOSFET is usually used as a bypass switch. By selecting a MOSFET switch with a low on-resistance the voltage drop due to its inherent on-resistance can be kept to a minimum. Unfortunately, MOSFET switches exhibit parasitic capacitances that must be considered at high speed. Charge injection of the MOSFET creates a voltage peak, when it is switched off at the end of the bypass mode. The settling takes time and prolongs the measurement period. This peak can cause momentary voltage drops of 5-10%, which can affect the operation of the DUT at high speeds. The challenge is how to cope with these parasitics that cause undesired clock feed-through and hence to avoid the switched circuit to be affected by the control signal.

[0005] Many charge injection cancellation techniques have been found so far. They are mostly based on a dummy switch or capacitor, such as for example in document EP-A-811850. These solutions are described in detail in the documents :

- "On Charge Injection in Analog MOS Switches and Dummy Switch Compensation Techniques", C.Eichenberger, W.Guggenbuhl, IEEE Transactions on Circuits and Systems, pp. 256-264, vol. 37, No. 2, Feb. 1990.
- "Dummy Transistor Compensation of Analog MOS Switches", C.Eichenberger, W.Guggenbuhl, IEEE Journal of Solid-State Circuits, Vol. 24, No. 4, pp. 1143-1146, August 1989.

[0006] The dummy is usually driven by an opposite clock and so it compensates the charge injection by the opposite charge injection, which results in the cancellation. The main disadvantage is that the

cancellation strongly depends on proper matching and actual type of MOSFET. These techniques cannot be applied in designs with discrete components, because single components have a much higher dispersion of parameters than matched on-chip components.

[0007] Another problem of existing I_{DDQ}-monitors is related to the sensitivity of these test devices. The background leakage current ($I_{Background\ Leakage}$) of deep sub-micron devices increases drastically as process technologies are decreasing in size and the number of transistors contributing to the background leakage is increasing drastically, whereas the order of magnitude of the defect current ($I_{Defect\ Leakage}$) remains more or less constant:

$$I_{Total\ Leakage}\ (\nearrow) = I_{Background\ Leakage}\ (\nearrow) + I_{Defect\ Leakage}\ (\rightarrow)$$

In order to distinguish the small defect leakage component from the background leakage current, the measurement resolution must be very high throughout the measurement range of the monitor. People skilled in the art know that increasing the measurement range is always done at the expense of measurement resolution. Yet the resolution should remain constant as the defect leakage current remains constant. Existing I_{DDQ} monitors do not offer a solution to this problem.

Aims of the invention

[0008] The present invention aims to provide a device for I_{DDQ} monitoring of electronic devices, which has a high resolution for higher I_{DDQ} levels, and which comprises means to reduce the influence of parasitic capacitances of the bypass switch. The device of the

application is capable of being used both in on-chip and off-chip applications.

Summary of the invention

[0009] The present invention is related to a device for measuring the supply current (I_{DDQ}) to an electronic device under test DU , which is powered by a supply voltage (V_{DUT}), said measuring device being placed in a supply line between said supply voltage and said device under test, said measuring device comprising a current measuring unit CMU, a current bypass unit or CBU in parallel to said CMU, said CBU comprising a power MOSFET in the path between said supply voltage (V_{DUT}) and said DUT, said CBU further comprising means to receive a clock signal, being a succession of high and low states, said CBU comprising two transistors connected by a series connection, which receive said clock signal at their gates or bases, and wherein the gate of said MOSFET is connected to said series connection, characterized in that a connection is present between one terminal other than the gate or base of one of said transistors in series, and either the source or the drain of said MOSFET.

[0010] According to a first embodiment, said two transistors are respectively a P-MOS transistor and an N-MOS transistor.

[0011] According to a second embodiment, said two transistors are bipolar transistors, respectively a PNP transistor and an NPN transistor.

[0012] Said two transistors in series may be arranged as an inverter or as a follower driver.

[0013] Said CBU may further comprise a diode, coupled in parallel to said MOSFET switch.

[0014] The invention is equally related to a device for measuring the supply current (I_{DDQ}) to an electronic

device under test, which is powered by a supply voltage (V_{DUT}), said measuring device being placed in a supply line between said supply voltage and said device under test, said measuring device comprising a current measuring unit or CMU, a current bypass unit or CBU in parallel to said CMU, characterized in that said measuring device further comprises an offset current device, said offset current device comprising a current source, for providing a constant offset current to said DUT.

[0015] Said current source is preferably programmable. It may be coupled in parallel to said current measuring unit, or it may be powered by a supply voltage (V_{DD}) which is different from the DUT supply voltage (V_{DUT}).

[0016] Any device according to the invention may further comprise a processing unit, which is in connection with said current measuring unit and with an output device and which is able to acquire an I_{DDQ} measured value from the CMU, characterized in that the processing unit is able to perform processing actions on said measurement.

[0017] Said processing actions are preferably chosen from the group consisting of :

- subtracting a measured I_{DDQ} value from a reference value or vice versa,
- comparing a measured I_{DDQ} value with a reference value and producing a pass/fail signal on the basis of the result of said comparison,
- subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value
- comparing a calculated value, resulting from subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value or vice versa, or from subtracting a measured I_{DDQ} value from a reference value or vice versa, with a

reference value and producing a pass/fail signal on the basis of the result of said comparison.

[0018] A device of the invention may be separate from said device under test, or it may be incorporated into said device under test.

Short description of the drawings

[0019] Fig. 1 represents a schematic view of an I_{DDQ} monitor according to the invention.

[0020] Fig. 2 represents illustrates the parasitic capacitances C_{gd} and C_{gs} of a power MOSFET transistor.

[0021] Fig. 3 illustrates the principle of a sample-hold circuit.

[0022] Fig. 4 illustrates a bypass switch, such as it is used in state of the art applications.

[0023] Fig. 5 shows four embodiments of a bypass switch according to the present invention.

[0024] Fig. 6 illustrates the result of a simulation-based comparison between a bypass switch of the prior art and a bypass switch of the invention.

[0025] Fig. 7 represents a device according to a preferred embodiment of the invention.

[0026] Fig. 8a and 8b represents graphs illustrating the effectiveness of the charge compensation obtained by the invention.

[0027] Fig. 9a and 9b represent schematic views of two embodiments of the current offset unit according to the invention.

[0028] Fig. 10 represents a graph, illustrating the application of a virtual measurement window to the leakage current, by using a monitor according to the invention.

[0029] Figures 11 to 14 illustrate different off-chip and on-chip embodiments of a device according to the invention.

Detailed description of the invention

[0030] Figure 1 illustrates a schematic view of an I_{DDQ} monitoring device or simply named 'monitor' 1, according to the invention. In this figure, the monitor is represented as a separate device, which can for example be incorporated into the test equipment, as a load-board application. It is emphasized that the same monitor can be designed as an on-chip device.

[0031] The monitor 1 is connected by two terminals 2 and 3, between a supply voltage source 4, and the Device-Under-Test DUT 5. The supply voltage V_{DUT} at the terminal 2 should be present also, with a minimum error, on the terminal 3, in order to create a maximum transparency of the monitor 1.

[0032] The measurement of the I_{DDQ} is performed by the current measuring unit CMU 6, during a non-switching state of the DUT. Test vectors 7 are applied to the DUT at a given clock frequency, by the test equipment 8. The CMU 6 may be a unit working according to the stabilized voltage source principle or any other prior art measurement method. A current bypass unit CBU 20 is placed parallel to the CMU 6. The CBU 20 preferably comprises a power MOSFET which can be closed prior to the occurrence of the transient peak resulting from the DUT's switching action. This transient peak occurs when a test vector is applied to the DUT or when the application of a clock cycle of the DUT's operational clock causes the DUT to change state. In between transient peaks and for the desired measurement states, the MOSFET is normally opened in order to send the quiescent current I_{DDQ} through the current measuring unit CMU 6.

[0033] The CBU 20 of the invention is new and inventive with respect to the prior art, and described in

more detail in the following paragraphs. Another block 21 may be present in the I_{DDQ} monitor of the invention. This is an offset current unit OCU 21, characteristic to the present invention and described at length further in this description. The operation of the CBU 20 and OCU 21 is controlled by the processing unit 9, via control signals 10 and 11. In particular, the PU 9 controls the opening and closing of the MOSFET incorporated in the CBU 20, on the basis of a clock signal derived from the clock with which the DUT is operated. The clock applied to the CBU is dependent on the relevant measurement sequence : there is not necessarily a measurement during every clock cycle of the DUT. When in measurement mode, the current measuring unit performs an I_{DDQ} measurement, during a non-switching period of the DUT and delivers a signal 12 related to the I_{DDQ} level, to the processing unit 9, which digitises the signal, and transmits it via the terminal 13, to the test equipment 8.

[0034] The test equipment 8 controls the processing unit 9, and processes the monitor's output 12, so that the result of the I_{DDQ} measurement is displayed on a screen. In the preferred set-up, the source 4 is not separate, and the supply voltage V_{DUT} is equally supplied by the test equipment 8. The displayed result is at least a pass/fail statement based on the comparison between the measured I_{DDQ} value and a predefined reference, often completed by the measured value of I_{DDQ}. Other measurement modes can be selected when using the preferred version of the processing unit 9. For example : the measurement of current signatures or a delta I_{DDQ} measurement mode wherein subsequent measurements are subtracted and the delta-values obtained are memorized and compared to a reference.

[0035] According to a preferred embodiment of the invention, the PU 9 itself performs the processing of the

incoming signals, for example the subtraction of two subsequent I_{DDQ} measurement values, before a result is transferred to the test equipment 8. Some examples of measurement modes, performed by a PU according to this embodiment, are given further in this description.

[0036] As mentioned already, the CBU 20 comprises a switch, preferably a power MOSFET with a low R_{ON} resistance, aimed at bypassing the I_{DDQ} measurement unit during the transient peaks of the supply current drawn by the DUT 5. Such a MOSFET, together with the loading-decoupling capacitance C_H, creates a generic sample/hold circuit. The CBU of the invention comprises new and inventive means to compensate for charge transfer phenomena.

[0037] A simplified high-speed model of a MOSFET switch 22 involves an on-resistance R_{ON} and two parasitic gate capacitances C_{gd} and C_{gs} as shown in figure 2. The resistance in the off-state can be considered infinite. The parasitic capacitances can reach values significantly higher than 1 nF in case of discrete power MOSFETs, but a typical value is in order of pF or less.

[0038] During MOSFET switching, a charge is injected from the gate through the drain and the source via C_{gd} and C_{gs}. Therefore the load connected to the drain or the source is directly affected by the control signal (clock) applied to the gate. The charge injection is not so important for MOSFET switches in digital circuits, but it is a dominant issue for analogue switch applications especially for sample/hold circuits (S/H). The generic S/H circuit (figure 3) involves an input voltage source V_{IN}, which is sampled by the MOSFET switch 22 and held by the hold capacitor C_H.

[0039] The sample/hold mode is controlled by the clock signal V_{CLK}, which is applied to the gate of the

switch. In the ideal case, the voltage at C_H would be the same as the sampled input voltage V_{IN}. In reality however, the change of the gate voltage invokes a change of parasitic C_{gs} charge, which is injected to C_H. Naturally, the change of C_H charge results in the change of the hold voltage across the hold capacitor so that this sampled value is not equal to V_{IN}. The actual error depends on the ratio between C_H and C_{gs}. C_{gs} and C_H are connected in series from the gate point of view. The C_{gd} parasitic capacitance can be neglected in this case, since this is discharged through V_{IN}, which is considered to be of low impedance.
The total gate capacitance referred to ground is

$$C_g = \frac{C_{gs} \cdot C_H}{C_{gs} + C_H}, \tag{1}$$

while the charge injection is $\Delta Q = C_{gs} \cdot \Delta V_G$ and similarly $\Delta Q = C_H \cdot \Delta V_H$.

Therefore, the hold voltage error is

$$\Delta V_H = \frac{C_{gs}}{C_{gs} + C_H} . \Delta V_G \tag{2}$$

and this can be further simplified for $C_H >> C_{gs}$

$$\Delta V_H = \frac{C_{gs}}{C_H} . \Delta V_G \, . \tag{3}$$

[0040] The formulas above assume the simplified model with a constant C_{gs} value. In reality, C_{gs} is a function of the voltage across the gate and the source. The on-state capacitance is higher than the off-state capacitance. As long as the MOSFET is in the on-state, the charge injection is eliminated by the on-resistance. The C_{gs} causes the injection mainly when the MOSFET is being switched off.

[0041] Figure 4 shows a normal uncompensated S/H with an inverter, comprising P-MOS and N-MOS transistors 23 and 24 respectively, connected by a series connection 30.

This inverter drives the switch's gate in a traditional way. The clock pulse 50 is synchronised with the DUT's operational clock. The inverter makes sure that during a high state of the pulse 50, the gate of the MOSFET 22 is low, i.e. the MOSFET is open (CBU off, measurement mode). When the clock signal 50 goes low, the MOSFET's gate goes high, i.e. the MOSFET is closed (CBU on, bypass mode). The transistors 23 and 24 are respectively off and on during a high clock pulse and vice versa during a low clock pulse, thereby changing the gate voltage at point 28 between a low and high value, so as to switch the MOSFET 22 off and on alternately. When used in an I_{DDQ} monitor, the voltage V_{IN} is the V_{DUT} voltage, and V_{DD} is an external supply voltage of the CBU. The high gate voltage, applied during a low state of the clock signal 50, is virtually equal to the driver supply voltage V_{DD}. Naturally, V_{DD} must be high enough to switch the MOSFET 22 on. When the clock 50 goes high, in order to open the MOSFET 22 (i.e. to switch it off), the MOSFET gate voltage is referred to ground and driven below the V_{HOLD} level, which is virtually equal to V_{IN}. This is the drawback, because the charge is fully transferred to the hold capacitor C_H, due to the high gate voltage change ΔV_G that takes place upon opening the MOSFET switch 22 (see formula (3) above).

[0042] Figure 5a to 5d show the structure of the CBU according to several embodiments of the invention. In the design of figure 5a, the gate voltage at 28 is referred to the source at point 29, instead of ground. To be more exact, the source of the N-MOS driver (transistor 24) is connected by connection 51 to the source of the MOSFET switch 22 instead of ground. The gate voltage level of the MOSFET 22 never drops below the MOSFET's (22) source voltage level. Thus, the change of the gate voltage ΔV_G is

limited, which results in a lower charge injection and thus a lower hold voltage error ΔV_H. During switching-off, the parasitic C_{gs} is being discharged directly between the gate and source of the MOSFET, so it does not affect the hold capacitance so much. In the design of figure 5a, both transistors of the driver inverter are in on-state for a while during the switching activity, which slightly charges the C_H from the supply V_{DD}.

[0043] The embodiment shown in figure 5b does not suffer from this slight drawback. Here, a follower driver is used in stead of the inverter. The P-MOS 23 and N-MOS 24 have changed places, meaning that the MOSFET's gate 28 is now high during a high clock signal and low during a low clock signal. The particular operation of a driver follower, which is known to the person skilled in the art is such, that the driver transistors are not switched on together during the switching of the MOSFET. This allows a further minimisation of the charge transfer.

[0044] Figure 5c is showing another embodiment. Once again, an inverter 23,24 is driving the MOSFET. Now however, the source of the N-MOS 24 is connected via connection 51, to the drain of the MOSFET 22, in stead of the source. The effect is however the same. The gate voltage of the MOSFET never drops below V_{IN}, which is virtually equal to V_{HOLD}. Furthermore, during the opening of the switch, the R_{ON} resistance is still momentarily low, before reaching a theoretically infinite value R_{off}. R_{off} is only really established as soon as the MOSFET gate voltage drops below the threshold voltage. A short resistive transition time occurs, before the resistance reaches its 'infinite' value. During this transition, a connection is effectively established between the source of the MOSFET, through R_{ON} and connection 51, to the source of the N-MOS

24, yielding the same effect as the design of figure 5a. Fig. 5d finally shows the switch of figure 5c, equipped with a follower driver, in stead of an inverter.

[0045] The circuits of figures 5a and 5b were simulated using SPICE. Figure 6 is a simulation result for the discrete MOSFET switch 22 of type BUZ 11, while the driver transistors 24 and 23 are BS170 and BS250 types respectively. The voltages are V_{DD} = 10 V, V_{IN} = 5 V, C_H = 100nF, the sample and hold periods are set to 100 μs. The sampling error is approximately 0.25 V in case of uncompensated S/H (curve 25), while the compensated inverter and follower configurations exhibit a much reduced error (curves 26/27). Curve 26 is relevant to the switch of figure 5a; curve 27 is relevant to the switch of figure 5b. In case the switch of figure 4, i.e. without compensation, is used as a current bypass unit in an I_{DDQ} monitor, the voltage drop at the DUT side will be in the range of 5-10%. This voltage drop can cause the DUT to malfunction or might result in data loss in memory elements. A compensated switch causes the DUT voltage to increase slightly, 0.5-1.0%. However, this is less harmful for the DUT operation.

[0046] Since this approach is versatile, error reduction (cancellation) factors of 8 to 30 times were reached under various conditions - for different input voltage V_{IN}, with different transistors etc. The only requirement is that the driver transistors must be much smaller (with much lower parasitic capacitances) than the sample switch. Similar results were reached with on-chip transistors. Models used CMOS technology ES2 1.5 μm with dimensions of 1000 μm/5 μm for MOSFET switch and 20 μm/5 μm for the driver transistors.

[0047] Figure 7 shows a preferred embodiment of the CBU 20 according to the invention. The CBU is represented as the device 20, shown in combination with a current measuring device that works according to the stabilized voltage drop principle, known in the art. The thus employed CBU reduces the peaks approximately five to ten times in comparison with an uncompensated bypass switch and therefore the settling is improved. There is no significant voltage drop on the V_{DUT} node thanks to the compensation circuitry. The circuit is a variant of the one shown in figure 5d, in that bipolar transistors 31(PNP) and 32(NPN) are used in stead of PMOS/NMOS transistors. The clock signal 50 is applied to the bases of both transistors, via protection resistances 34 and 35. The collector of the PNP transistor 31 is connected to the drain of the MOSFET 22, by connection 51. This makes this switch equivalent to the one shown in figure 5d. The rest of the circuitry, including the sensing opamp 36, the instrumentation opamp 37 and the comparator 38, are part of the Current Measuring Unit (CMU), working according to the stabilized voltage drop principle, such as it is known in the art, and delivering a pass/fail signal 39. The same type of compensated switch can be used in combination with other types of CMU.

[0048] If the gate of the bypass MOSFET switch 22 would be connected directly to the output of the CMOS logic at V_{DD}, or if the PNP transistor's collector would be connected to ground, the gate voltage of the MOSFET 22 would be referred to ground and driven below the V_{DUT} level and the charge would be fully transferred to the capacitor C_H, when the bypass switch is opened. The compensation consists of the two bipolar transistors 31 and 32. When the bypass is being switched off, the gate is pulled down to V_{DUT} instead of ground by the PNP transistor 31. As a

result, C_H is much less affected by the charge injection. The NPN transistor 32 enables to switch the MOSFET on. Both compensation bipolar transistors require no matching and they can be replaced by MOSFETs with low parasitics.

[0049] In the embodiment of figure 7, the switch further comprises a diode 52. This is preferably a Schottky diode. Its function is to avoid excessive loss of supply voltage to the DUT, when the MOSFET is in bypass mode. This may occur as a consequence of abnormally high peaks in the supply current flowing through the MOSFET, and causing a possible voltage drop, despite the MOSFET's low R_{ON} resistance. The diode 52 allows to clamp the supply voltage to the DUT at a stabilized value.

[0050] The MOSFET 53 is not a part of the CBU 20. It's function is to work as a sample and hold switch, allowing to eliminate noise from the signal appearing at the input of Opamp 36, during measurement mode.

[0051] The graphs in figures 8a and 8b illustrate the effect of the compensation obtained by the CBU of the invention. Figure 8a shows a typical waveform of the clock pulse 50, wherein a high pulse corresponds to a bypass period, and a low pulse to a measurement period. The curve 60 shows the V_{IDDQ} level, which is a voltage present at the output of the instrumentation amplifier 37 (see figure 7), and which is directly related to the I_{DDQ} value. A valid measurement can only be acquired after the peak 61 has settled. Charge transfer effects described above tend to prolong this settling time. In figure 8b, a comparison is made between the settling of the curve 62, without charge compensation, and of curve 63, with charge compensation according to the invention. The settling time is clearly reduced.

[0052] Block 21 shown in figure 1 is equally a characteristic element of the invention. This is the

Offset Current Unit (OCU). As the large background leakage current does not contain any defect information, it is not practical to measure this component of the leakage current. In practice, the background leakage current can be of the order of 100mA, while the defect-related leakage current $I_{DDQdefect}$ is typically between 0 and 10mA. The background leakage component can therefore be regarded as an offset current ($I_{DDQoffset}$). The total quiescent current I_{DDQ} is the sum of both previously described components.

$$I_{DDQ} = I_{DDQBackground} + I_{DDQDefect}$$

[0053] Measuring the totality of this I_{DDQ} current, requires a CMU with a high dynamic range, and thus reduced sensitivity. As stated above, this is a growing problem, due to increasing background leakage current in submicron devices, while the defect leakage current remains of the same order. The total I_{DDQ} level becomes too high for a current measuring unit, having a high resolution, as is desired for reasons of accuracy. It would therefore be advantageous if only the defect leakage component is measured. As shown schematically in figure 9, the OCU 21 is actually a current source 40, delivering an essentially fixed offset current into the supply line to the DUT. The current source will deliver a given offset current level $I_{DDQoffset}$ to the summing node 41, so that only the I_{DDQ} above this level is drawn from the current measuring unit 6. In that way a flexible virtual measurement window (VMW) 42 is created with a high measurement resolution (figure 10). The offset current source is preferably a programmable current source. The offset level 43 which is delivered as an offset current is programmable and variable during the measurement. It is basically controlled by the operator of the test equipment, through the processing unit 8. Two

embodiments are considered, as shown in figures 9a and 9b. In figure 9a, the current source 40 is connected to the supply voltage V_{DUT}, placing the OCU in parallel to the CMU. However, a parallel connection is not necessary. The offset current unit may for example be connected to the device supply voltage V_{DD} (figure 9b). Autoranging sequences are preferably performed prior to applying a series of test vectors, in order to establish the optimal level of the applied offset current. For this purpose, a programmable current source 40 is preferably used.

[0054] The offset current unit 21, possibly in combination with a compensated switch 20 according to the invention, can be applied in various ways. In the off-chip current measurement domain, the programmable current source 21 can be implemented either as a stand-alone module (figure 11) or it can be part of the off-chip current monitor 100 (figure 12). The block 100 in figures 11 to 14 represents an I_{DDQ} monitor with a CMU 6, and preferably with a CBU 20 according to the invention. The off-chip current monitor architecture is of no importance to the windowing concept. In the on-chip domain, again the offset current unit 21 can be an add-on core to the Built-In Current Sensor (BICS) (figure 13) or be part of the BICS itself (figure 14). The BICS architecture is of no importance to the concept. In all embodiments shown in figures 11-14, the dotted line delineates what is to be understood as the device 1 of the invention.

[0055] The (programmable) current source can be controlled by the ATE 8 (figures 11a, 12a, 13a, 14a) or by the on-chip/off-chip I_{DDQ} monitor (figures 11b, 12b, 13b, 14b) and although it is not necessary, the offset current unit can be part of a auto-windowing procedure.

Examples of measurement modes performed by the Processing Unit.

[0056] The following measurement modes comprise calculations which are performed by the processing unit itself. Results of calculations (subtraction of I_{DDQ} values, comparison results) are transferred to the ATE 8 which may further process them or display the results on a screen.

- Standard I_{DDQ} mode - I_{DDQ} measurements are made and compared against one predefined reference value resulting in a pass/fail result. Pass = measurement is below reference, Fail = measurement is above reference.
- Current signatures - this is a special version of the standard I_{DDQ} mode, for a current signature approach, I_{DDQ} measurements are made and compared against a predefined vector related pass/fail reference, resulting in a pass/fail result.
- Standard Delta-I_{DDQ} mode (vector-to-vector delta) - I_{DDQ} measurements are made, subsequent measurements are subtracted from each other (delta calculation). The measurement is preferably but not necessarily compared against a predefined absolute reference and the calculated delta is compared against a predefined delta reference value, resulting in a pass/fail result. Delta as well as absolute reference(s) can be set either globally or on a vector-to-vector basis.
- Vector to reference vector Delta-I_{DDQ} mode - A reference vector is selected of which the related I_{DDQ} measurement serves as reference for the following measurements. Typically the reference vector is the first I_{DDQ} vector (this situation is supported by the standard vector to reference vector delta I_{DDQ} mode

firmware). I_{DDQ} measurements are then made, the measurement result of each subsequent measurement is subtracted from the reference value gathered during the reference vector measurement (delta calculation). The measurement is preferably but not necessarily compared against a predefined absolute reference and the calculated delta is compared against a predefined delta reference value, resulting in a pass/fail result. Delta as well as absolute reference(s) can be set either globally or on a vector-to-vector basis.

- Pre and Post stress Delta-I_{DDQ} mode - A first set of I_{DDQ} measurements are made (pre stress), then stress is applied to the device under test, followed by a second set of I_{DDQ} measurements (post stress). The results from the corresponding pre and post stress measurements are subtracted (delta calculation). The measurement is preferably but not necessarily compared against a predefined absolute reference and the calculated delta is compared against a predefined delta reference value, resulting in a pass/fail result. Delta as well as absolute reference(s) can be set either globally or on a vector to vector basis

CLAIMS

1. A device (1) for measuring the supply current (I_{DDQ}) to an electronic device under test DUT (5), which is powered by a supply voltage (V_{DUT}), said measuring device (1) being placed in a supply line between said supply voltage and said device under test (5), said measuring device comprising a current measuring unit CMU (6), a current bypass unit or CBU (20) in parallel to said CMU, said CBU comprising a power MOSFET (22) in the path between said supply voltage (V_{DUT}) and said DUT (5), said CBU further comprising means to receive a clock signal (50), being a succession of high and low states, said CBU comprising two transistors (23/24 or 31/32) connected by a series connection (30), which receive said clock signal (50) at their gates or bases, and wherein the gate of said MOSFET is connected to said series connection (30), characterized in that a connection (51) is present between one terminal other than the gate or base of one of said transistors in series, and either the source or the drain of said MOSFET (22).

2. The device according to claim 1, wherein said two transistors are respectively a P-MOS transistor (23) and an N-MOS transistor (24).

3. The device according to claim 1, wherein said two transistors are bipolar transistors, respectively a PNP transistor (31) and an NPN transistor (32).

4. The device according to claim 1, 2 or 3, wherein said two transistors in series are arranged as an inverter.

5. The device according to claim 1, 2 or 3, wherein said two transistors in series are arranged as a follower driver.

6. The device according to any one of the preceding claims, wherein said CBU further comprises a diode (52), coupled in parallel to said MOSFET switch.

7. The device according to claim 1, further comprising a processing unit (9), which is in connection with said current measuring unit (6) and with an output device (8), and which is able to acquire an I_{DDQ} measured value from the CMU (6), characterized in that the processing unit is able to perform processing actions on said measurement.

8. The device according to claim 7, wherein said processing actions are chosen from the group consisting of :

- subtracting a measured I_{DDQ} value from a reference value or vice versa,
- comparing a measured I_{DDQ} value with a reference value and producing a pass/fail signal on the basis of the result of said comparison,
- subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value or vice versa,
- comparing a calculated value, resulting from subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value or vice versa, or from subtracting a measured I_{DDQ} value from a reference value or vice versa, with a reference value and producing a pass/fail signal on the basis of the result of said comparison,

9. A device (1) for measuring the supply current (I_{DDQ}) to an electronic device under test (5), which is powered by a supply voltage (V_{DUT}), said measuring device (1) being placed in a supply line between said supply voltage and said device under test (5), said measuring device comprising a current measuring unit or CMU (6), a current bypass unit or CBU (20) in parallel to said CMU,

characterized in that said measuring device (1) further comprises an offset current device (21), said offset current device comprising a current source (40), for providing a constant offset current to said DUT (5).

10. A device according to claim 9, wherein said current source (40) is programmable.

11. A device according to claim 9 or 10, wherein said current source is coupled in parallel to said current measuring unit (6).

12. A device according to claim 9 or 10, wherein said current source is powered by a supply voltage (V_{DD}) which is different from the DUT supply voltage (V_{DUT}).

13. The device according to claim 9, further comprising a processing unit (9), which is in connection with said current measuring unit (6) and with an output device (8), and which is able to acquire an I_{DDQ} measured value from the CMU (6), characterized in that the processing unit is able to perform processing actions on said measurement.

14. The device according to claim 13, wherein said processing actions are chosen from the group consisting of :

- subtracting a measured I_{DDQ} value from a reference value or vice versa,
- comparing a measured I_{DDQ} value with a reference value and producing a pass/fail signal on the basis of the result of said comparison,
- subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value
- comparing a calculated value, resulting from subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value or vice versa, or from subtracting a measured I_{DDQ} value from a reference value or vice versa, with a

reference value and producing a pass/fail signal on the basis of the result of said comparison.

15. A device according to any one of claims 1 to 8, wherein said device is separate from said device under test.

16. A device according to any one of claims 1 to 8, wherein said device is incorporated into said device under test.

17. A device according to any one of claims 9 to 14, wherein said device is separate from said device under test.

18. A device according to any one of claims 9 to 14, wherein said device is incorporated into said device under test.

ABSTRACT

DEVICE FOR MONITORING QUIESCENT CURRENT OF AN ELECTRONIC DEVICE

The present invention is related to a device (1) for measuring the quiescent current I_{DDQ} drawn by an electronic device such as a CMOS device or an IC, from a supply voltage. The quiescent current is drawn in between switching peaks, and is a measure for the quality of a device under test. The measurement device of the invention comprises a current measuring unit (6), and parallel to this CMU (6), a current bypass unit CBU (20), comprising a power MOSFET. In the CBU of the invention, a connection (51) is present between a terminal other than the gate or base of one driver transistor and the source or drain of the MOSFET, thereby minimising the charge transfer effects which are likely to occur during switching of the MOSFET. The invention is further related to a measurement device for IDDQ measurement comprising a current offset unit (21), which is aimed at improving the measurement range, without losing measurement resolution.

(Figure 1)

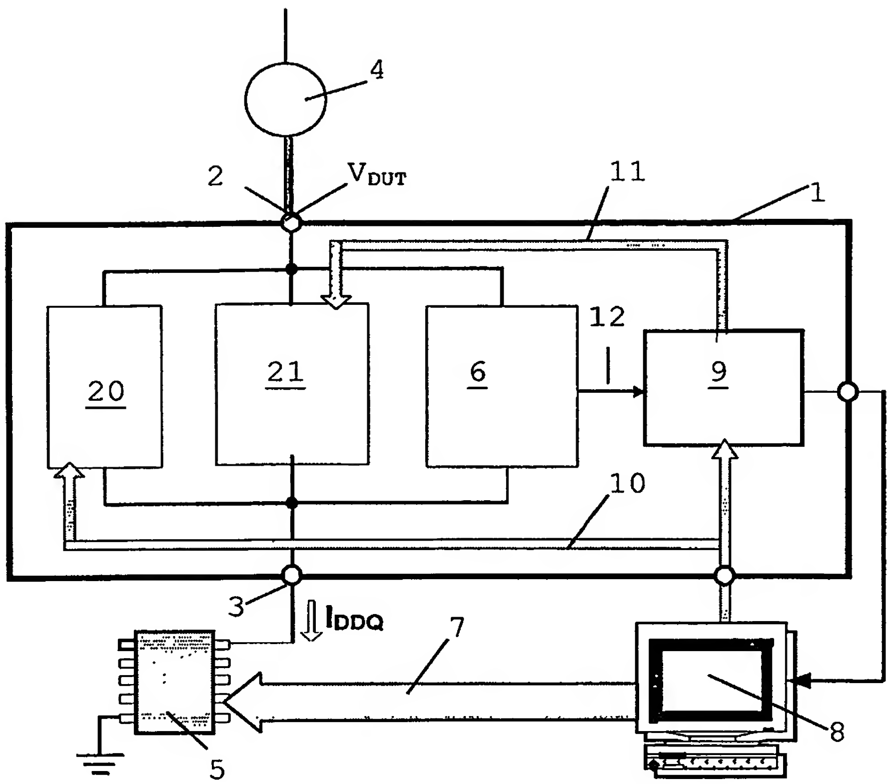
4
2
V_{DUT}
11
1
20
21
6
12
9
10
3
I_{DDQ}
7
8
5

FIG. 1

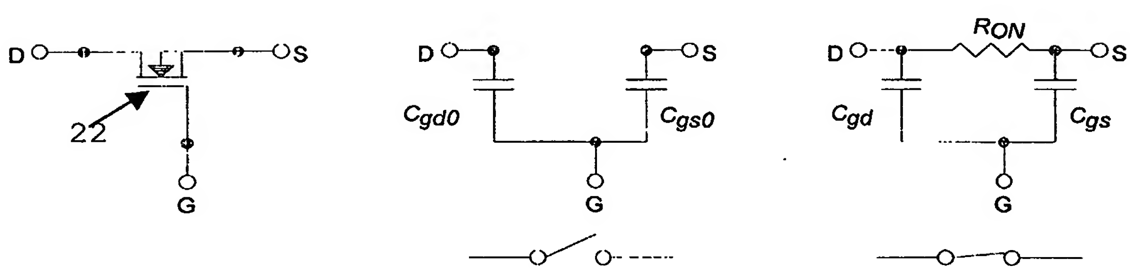
D
S
22
G
D
S
Cgd0
Cgs0
G
RON
D
S
Cgd
Cgs
G

FIG. 2

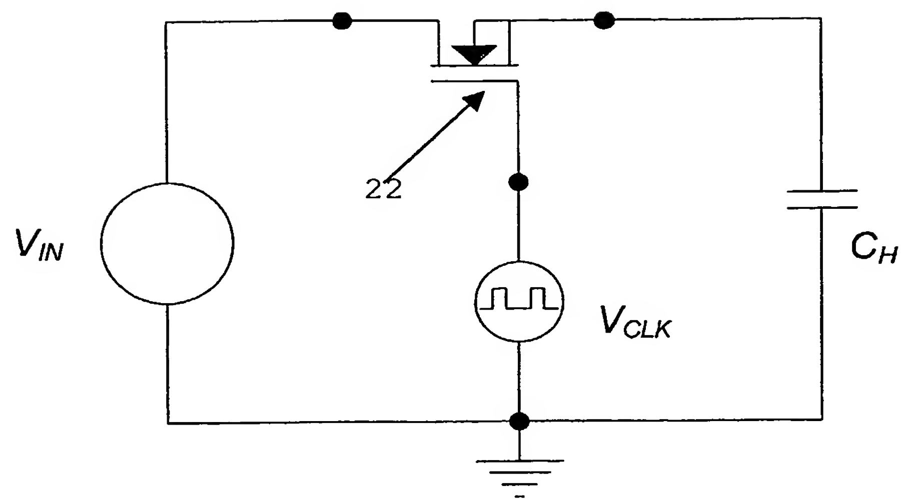

FIG. 3

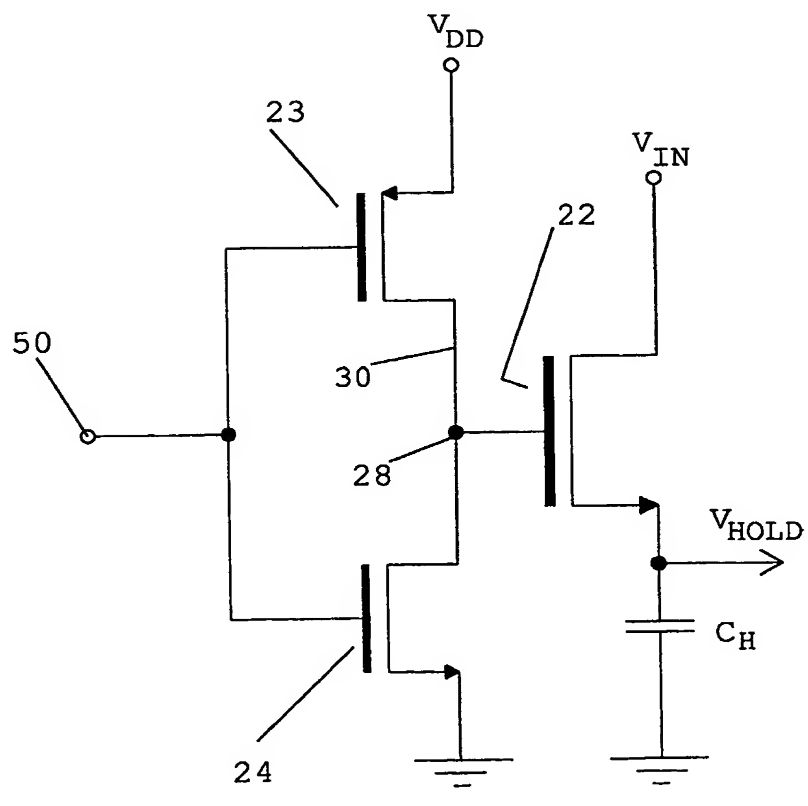

FIG. 4

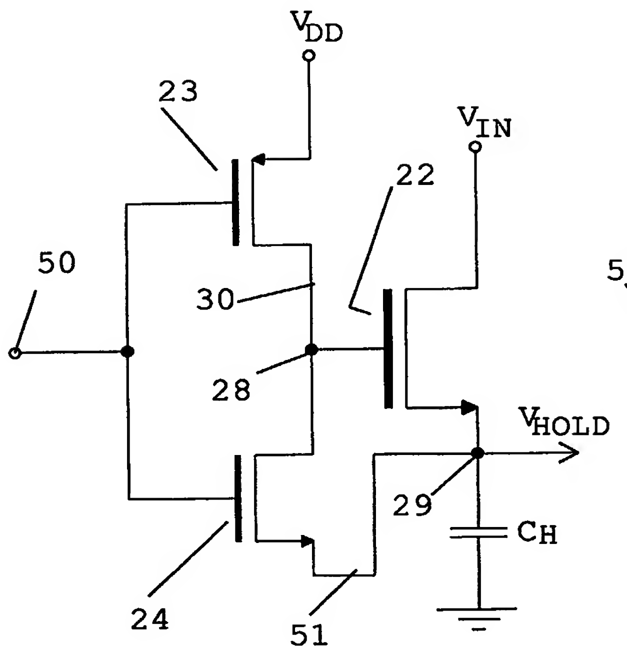

FIG. 5a

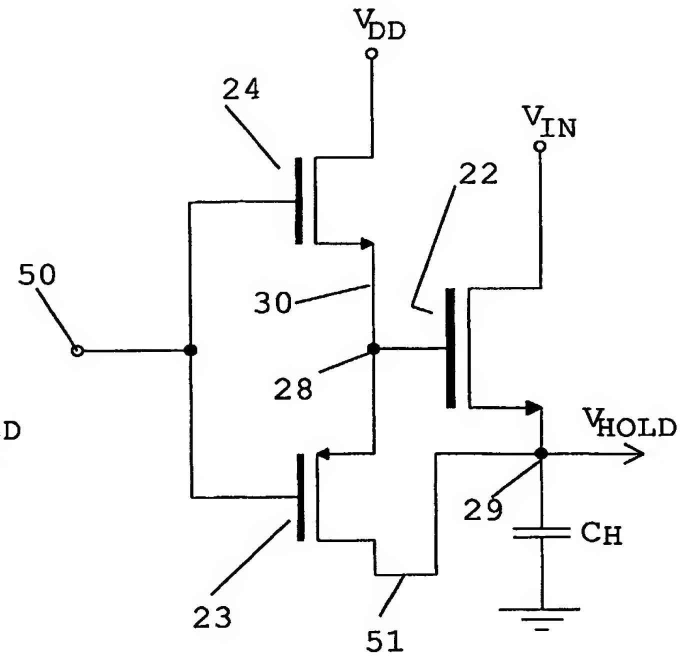

FIG. 5b

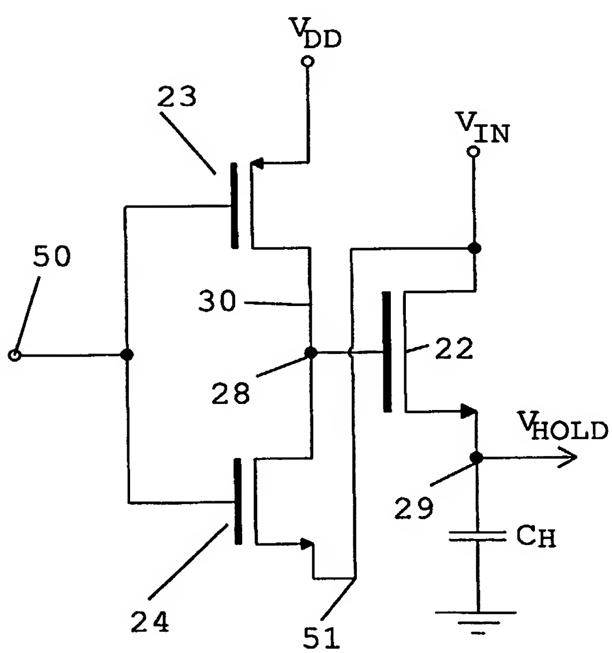

FIG. 5c

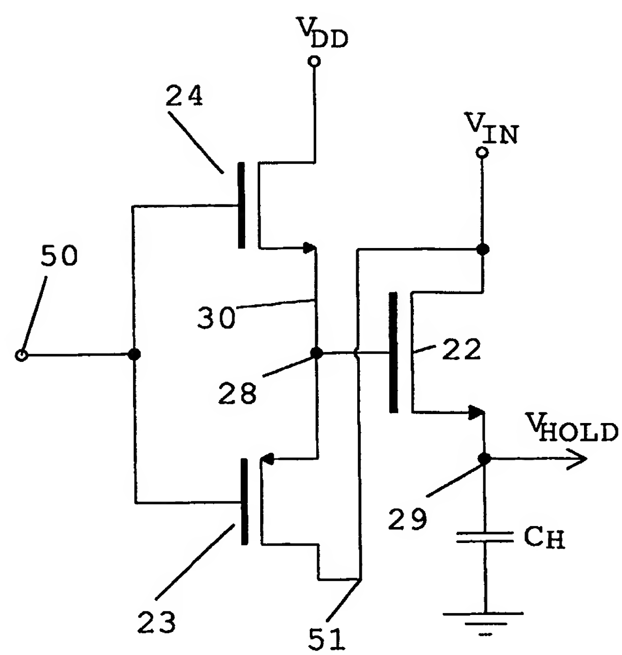

FIG. 5d

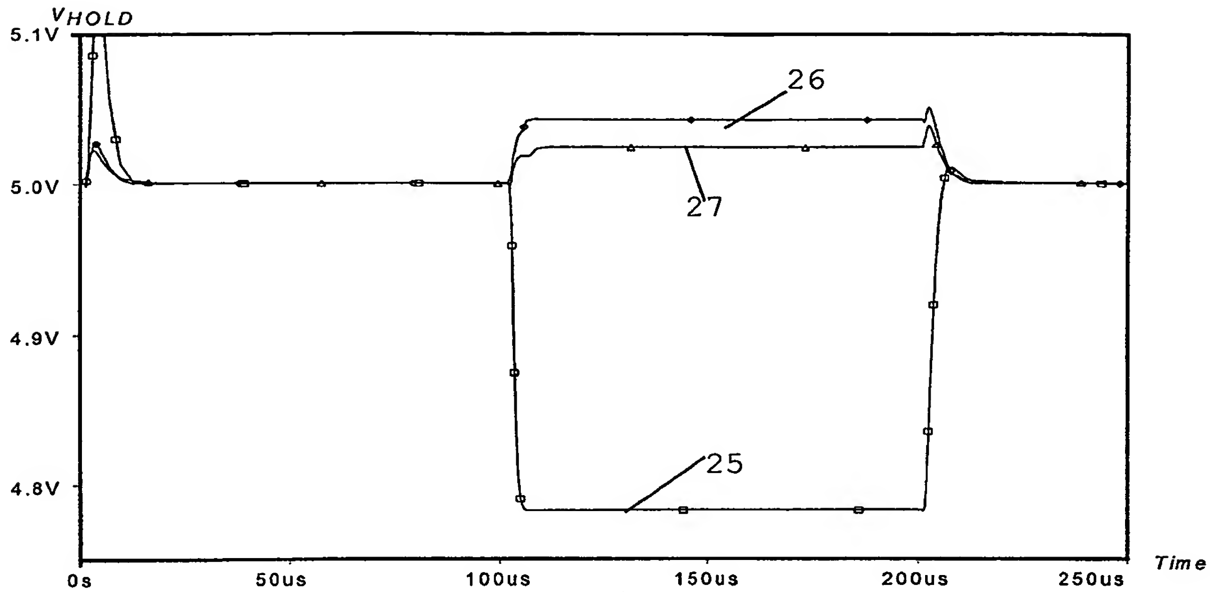
VHOLD
5.1V
5.0V
4.9V
4.8V
26
27
25
0s
50us
100us
150us
200us
250us
Time

FIG. 6

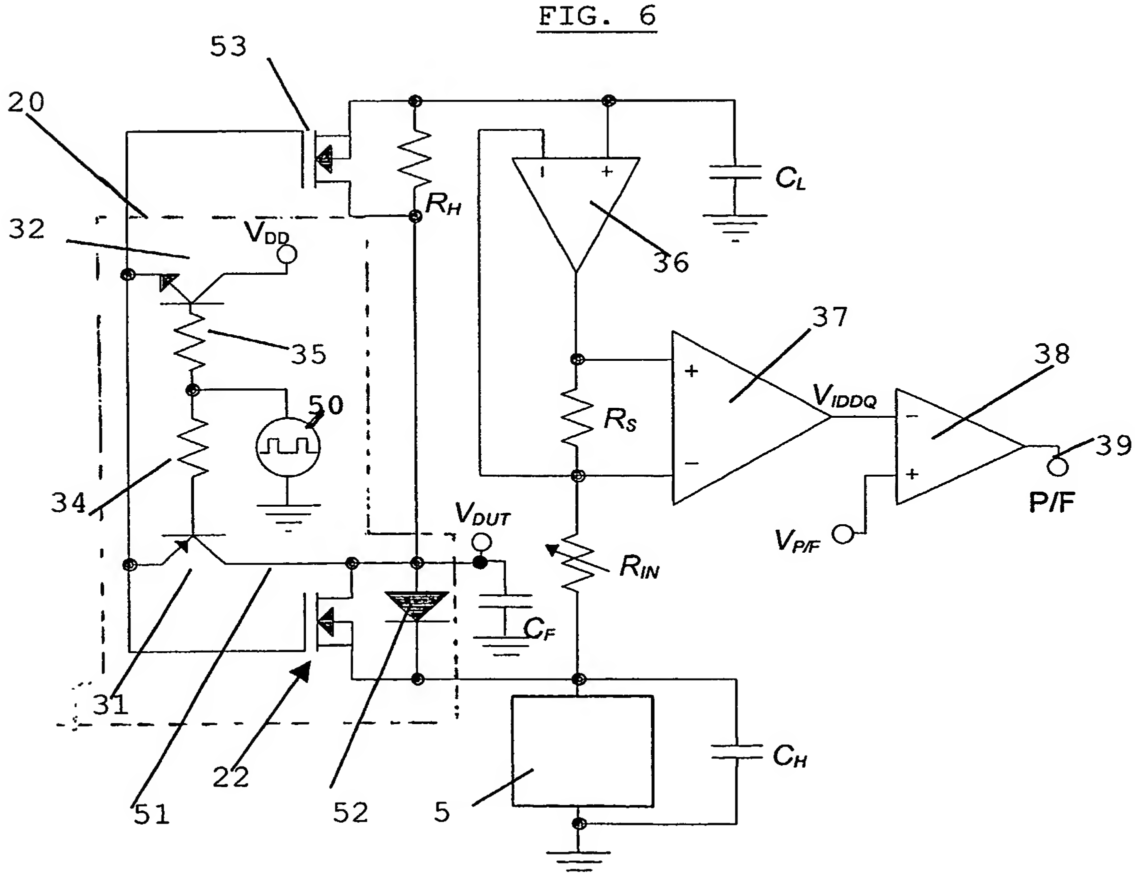
53
20
32
VDD
35
50
34
31
51
22
52
5
RH
36
CL
37
38
39
RS
VIDDQ
VDUT
RIN
CF
CH
VP/F
P/F

FIG. 7

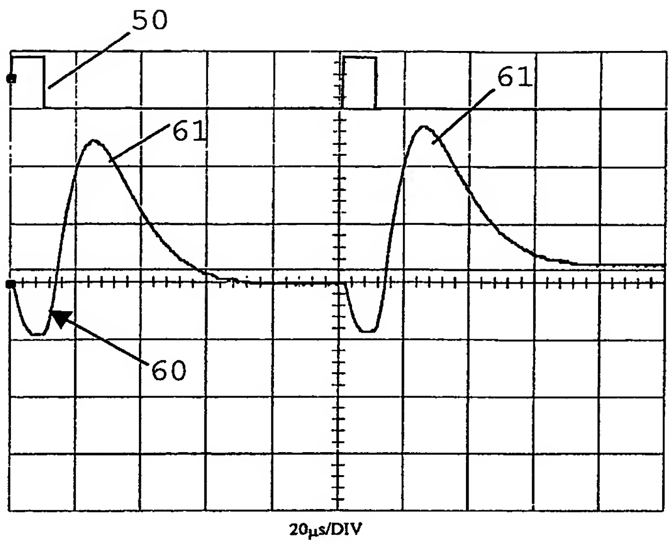

FIG. 8a

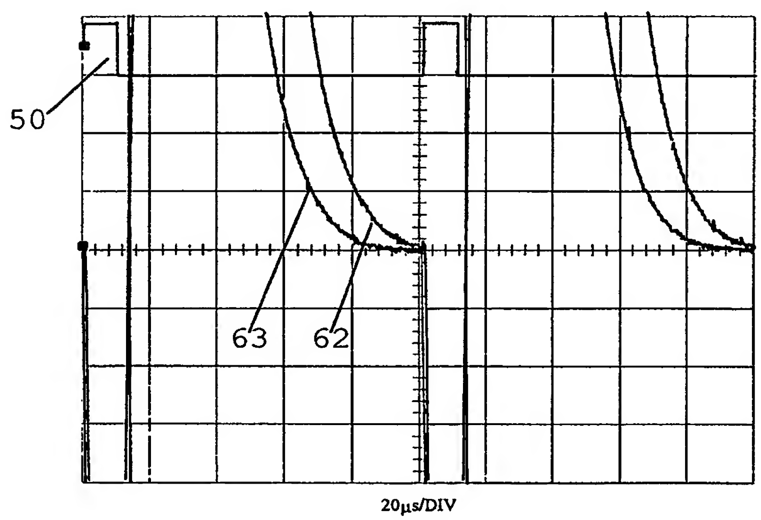

FIG. 8b

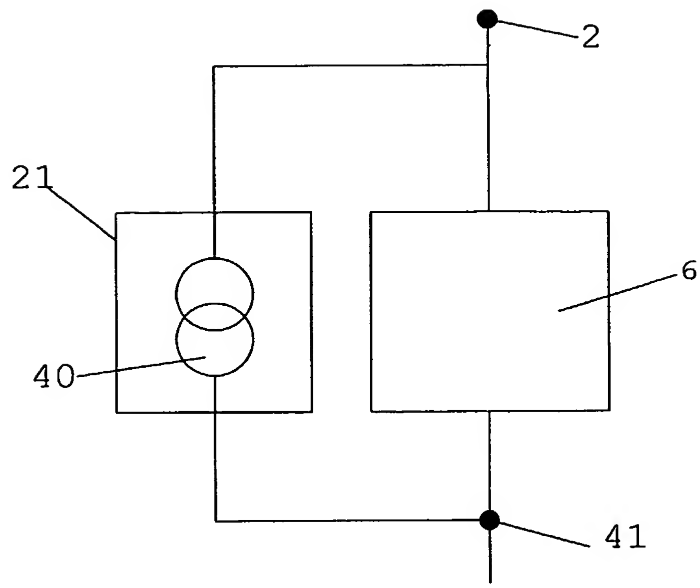

FIG. 9a

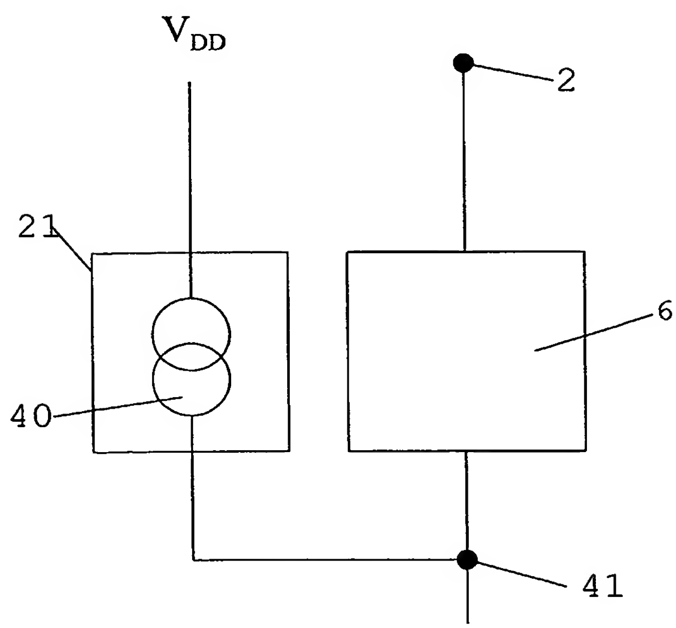

FIG. 9b

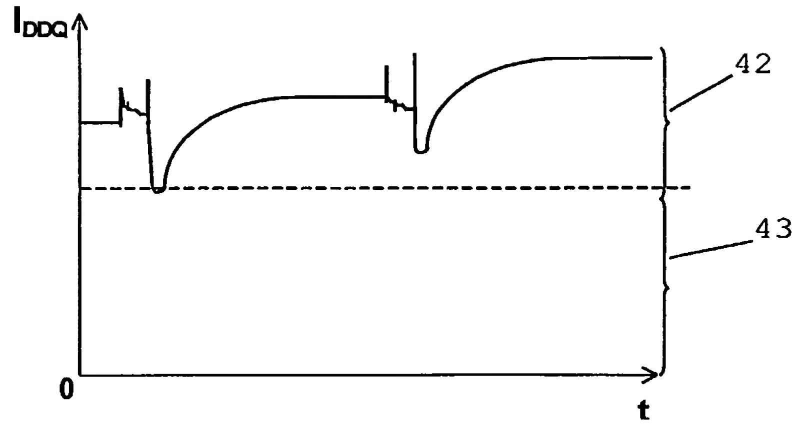

FIG. 10

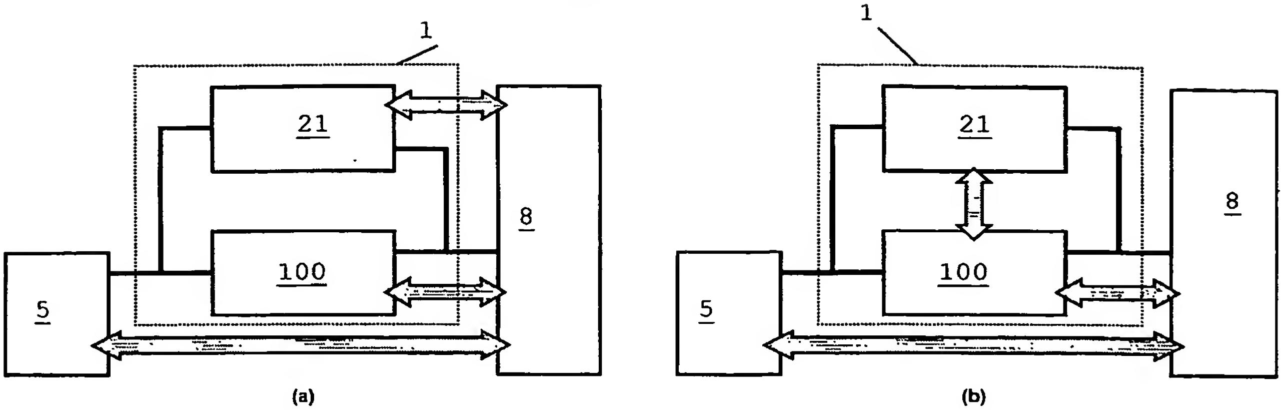

FIG. 11

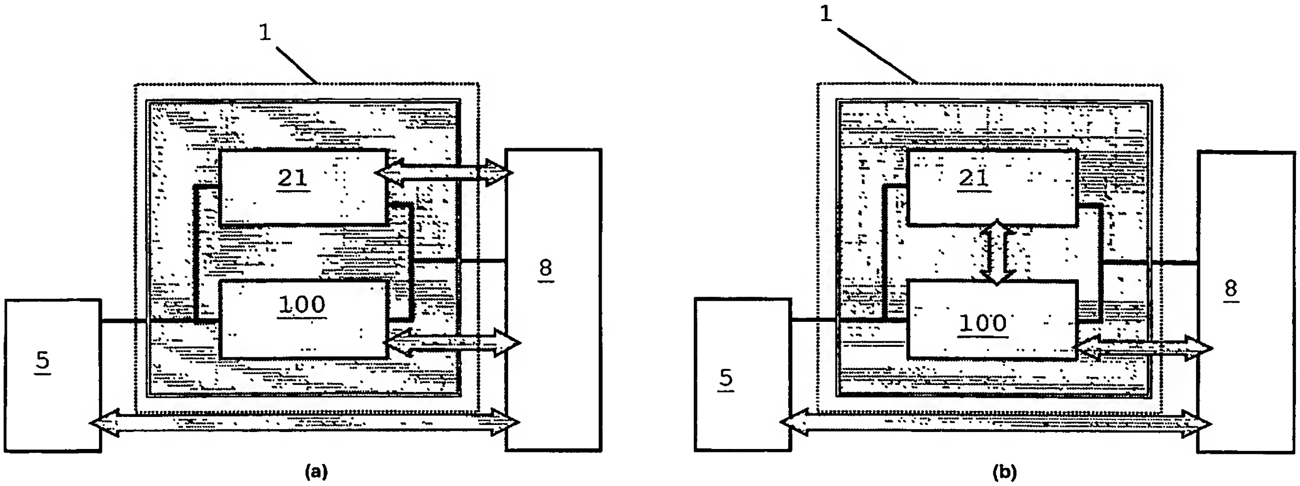

FIG. 12

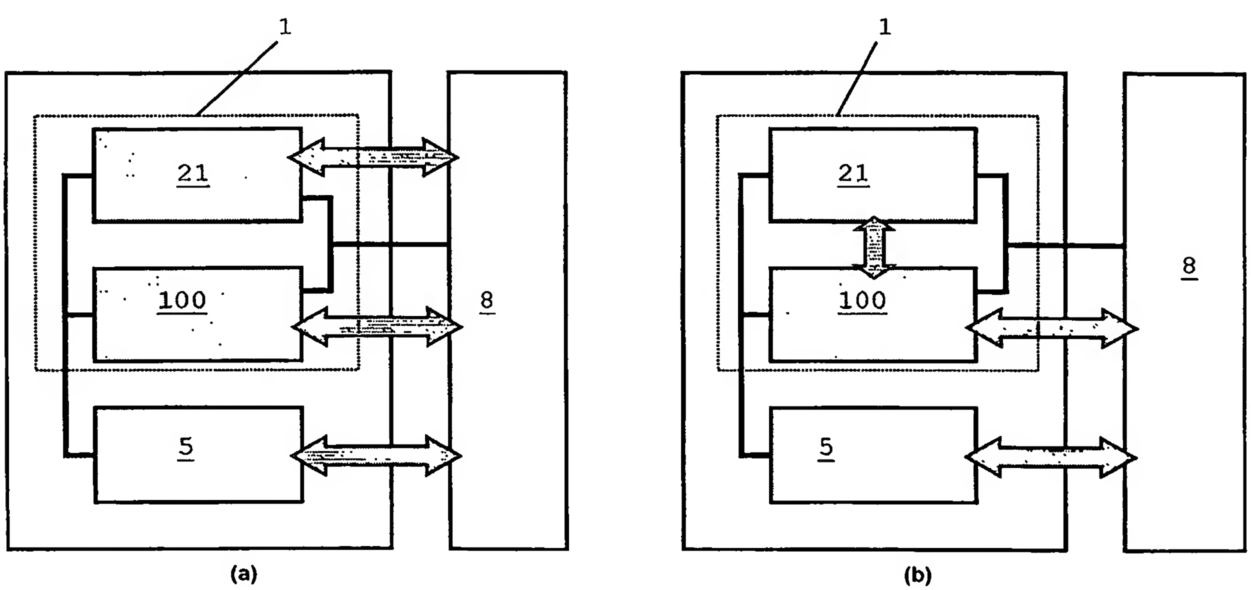

FIG. 13

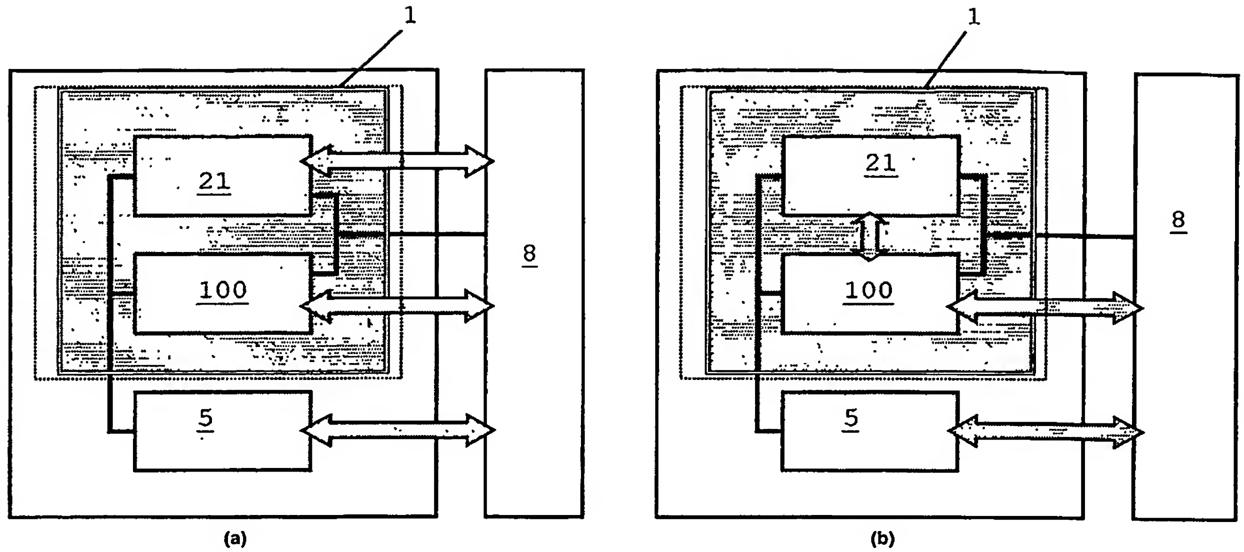

FIG. 14